Implementation of VLSI Based Router for Custom Network On Chip Applications

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Abstract: A fast full-chip synthesis method to construct network-on-chips (Custom Noc) for network on chip based systems. It can be used for irregular network topology for specific designs with already known communication demands. In this method processing elements and the communication architectures are to be synthesized simultaneously in the floor planning process, thus it is called Custom Noc process. CusNoc synthesizes in two steps. The desired network topology is generated first and it depends on already existed communication analysis. In this process, the Processing elements have to be partitioned into groups and a router is assigned to each group so the utility of routers can be maximum. So, the number of routers passed by a packet or hops is minimized, thus reduces power consumption. Finally, network topology is formed by properly connecting these groups. Here the router is a ‘Network Router’ that it has a one input port and the packet enters through this port. There are five output ports to where the packet can be driven out. Packet contain two parts and they are data (payload) and address sequence. The width of Packet which carries information is 8 bits and length of packet transferring may be from 1 to 32 bytes. It drives the packet to destination ports corresponds to the address sequence in the packet. Each output port contains 3-bit unique address. The switch drives the packet to the output port, when the destination address in the packet matches with any the output port address. The packets contain 5-bit data. In this paper uses Xilinx ISE tool for synthesizing and Modelsim for simulation.

Keywords: Router, Verilog, Finite State Machine, Look Up Tables.

1.INTRODUCTION

NoC topologies can be classified into two categories: regular and irregular. The CusNoC deals with irregular topologies. The performance of NoC based system depends upon the processing speed of PEs but also on quality of data transmission. The communication performance i.e., delay and power consumption is mainly decided by network topology and routing algorithm. It requires fewer network elements so it consumes less power to synthesize an irregular topology. The algorithm is very fast. Custom NoC is carried out in 2 steps in which the first one is the topology generation constrained by communication analysis followed by floor planning of Processors and group of routers. Routers are assigned according to communication demands. PEs are partitioned into groups where cores in same group share the common router. Hence the router utilization is maximized and it leads to fewer routers in NoC. The latency required for transmitting a packet is reduced by minimizing total number of hops required actually. Both PEs and network components are planned at the same time. The processes are carried out in two phases. In phase-I the isolated source PEs are removed in first step. In second step isolated target PEs are removed. Finally the subset successor tree is formed in which all source components and target components are grouped. In phase-II Router Sharing Graph clustering is carried out in four steps.

1. Communication Intensity Driven RSG Composition: The initial RSGs can be constructed in a way such that 100% router utility is achieved. The amount of communication required is Comm(acij)=SCiX TCj

2. Residual Component Connection: Each RSG is constructed by combining a source component and a target component. If number of SC and TC are not equal then some components will be left without joining any RSG. Such components are known as residual components. Residual component can be combined with an existing RSG if it has at least one successor belonging to an existing RSG. Otherwise a new RSG containing the residual component is created.

3. RSG Merging: In this step RSGs are merged in order to reduce the overall number of RSGs. By this fewer routers and fewer hops per message help reduction in power consumption. Two routers are merged if the maximum grouped I/O ports are 5.

A Router is a device which forwards data packets among various computer components. The hardware routers perform same basic tasks as ICs but
with even more features and functions than ICs. Broadband or Internet allow to share internet connected computers. Routing is the process of selecting best path in a network. Routing can be used to forwarding packets among network. It can be connected to two or more datalines from different computer networks. When data packets come in any of lines, then the router reads the address sequence in the packet determines its destination address. Then it uses information in routing table to direct the respective packet to next network.

II. PRINCIPLE

‘NETWORK ROUTER’ has one input port and through that port packet enters. It consists of 5 output ports to where packet has to be driven out. Packet consists of 3 parts. They are Header, Payload and Parity. The packet width is about 8 bits and the packet length varies between 1 byte to 32 bytes. There are 2 fifo devices allocated for each of five output ports, and they store the data which is coming from input port. The fsm router module generates the control signals to drive the packet to corresponding address. The ff_sync module provides synchronization between fsm_router module and 2 fifo’s. So each input port is able to communicate with 5 output ports.

PACKET-HEADER:

The Packet header consists of 2 fields and they are DA and length of packet. The DA field specifies the particular destination address of the packet which is of 3 bits. So based on DA the router drives the packet to corresponding destination port. Each output port contains its unique address and its of 3-bits. If the destination address of the packet matches with any of 5 output ports then it is driven to the respective output port. Length of data specifies the total number of data bytes which are carried out by the packet. A packet can have maximum data size of 32 bytes. The packet is driven by the switch to the output port. The data length is about 5 bits. Length is exact in terms of bytes. Data should be in terms of bytes.

III. OPERATION

The Five Port Network Router consists of three blocks. They are i. 8-Bit Register block, ii. Router Controller block and iii. output block. The router controller block uses Finite Machine States, here it contains six different states and 5 output ports which are having 2 FIFOs each combined together in output block. The FIFOs store data packets and those are retrieved back, when this data has to be send to anywhere then the data will be read from FIFOs. This paper using the global clock, reset signals and suspended data signals are the outputs of the router as shown in Fig.1. The FSM controller gives the SUSPENDED_DATA information also.

![Fig1: Block Diagram of Router Protocol.](image1)

The ROUTER may be operates with only one master device and but with one or more slave devices. The RE (read enable) pin is fixed to logic low if the slave permits it and there exists single slave. To initiate an action such as the mobile operators, that start conversion, few slaves require the falling edge. In case of multiple slave devices, an independent RE signal is required for both the master and slave.

![Fig2:FIFO Block](image2)

A. FIFO Block

The router design requires 2 fifos. The capacity of each fifo is of 8 bit width and 16 bit depth as shown in Fig.2. The fifo works on system clock. It contains a synchronous input signal reset to provide communication between fifo and fsm. If reset signal is low then it specifies that fifo_full is 0, fifo_empty is 1 and data_out from fifo is 0. In the Write operation, the data at data_in pin is sampled at rising edge of the clock, when input write_enb is high it indicates that fifo is not full. The Read Operation carries on at rising edge of the clock, the data can be read from output data_out, if read_enb is high it indicates that fifo is not empty. Both Read and Write operations can be done simultaneously.
B. Synchronous Block

Fig3: Synchronous Block.

ff-sync provides synchronization between fsm and fifo modules. It provides faithful communication between single input port and 5 output ports as shown in Fig.3. It will detect the address of channel and will latch it till packet_valid is asserted, address and to latching the incoming data into the fifo of that particular channel, write_enb_sel is be used. When fifo_full output signal is generated, then no data can be accepted by output protocol, and if fifo_empty output signal is generated then it indicates that fifo is ready to read the data. The output vld_out signal will be low if present fifo_empty goes low, it means that present fifo is ready to read. The write_enb_reg signal which arrives from the fsm generates write_enb signal for the present fifo that is selected by its address.

C. Router Register Block

This module consists of 3 set of registers and they are i. status registers, ii. data registers and iii. parity registers which are required for network router. All these registers can be latched on with rising edge of the clock as shown in Fig.4. Data is stored in the fifo when data registers latches the data from data input which depends on state of fsm and status control signals. Apart from it, data should be latched into the parity registers for parity calculation and this one is compared with the parity byte of the packet. If packet parity is not equal to the parity obtained in parity register then an error signal is generated. Internal parity register stores the obtained parity, which calculated by parity register for packet data, when packet is transmitted fully, the internal calculated parity is compared with parity byte of the packet. An error signal could be generated if packet’s parity is not equal to the internally stored parity. The “fsm_router” module is the controller circuit for the router. This module generates the control signals when new packet is sent to router. These control signals are used by other modules to send data to output and writing data into the fifo.

Fig4: Router Register Block.

Fig5: FSM Block.

Fig6: FSM State Diagram.
V. CONCLUSION

In this paper, a reduced area (NO OF LUT’S) of a five output port router is presented. The proposed router structure functionality is implemented in Verilog HDL and proven that this architecture consumes less resources in terms of no of LUT’S, slices and no of IO Buffers. This paper uses Xilinx ISE EDA Tool is used for synthesis and for simulation. The data that sent through the five output router is reached the destination with 9.375ns latency. In future it is possible to estimate the power consumption also.

VI. REFERENCES


